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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/550,642	04/14/2000	David F. Sorrells	1744.0920001	9236

7590 05/18/2005

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EXAMINER	
ODOM, CURTIS B	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/550,642	SORRELLS ET AL.	
	Examiner	Art Unit	
	Curtis B. Odom	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *75-81,83-92,94-104,106-115 and 117-123* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *75,76,79-81,83-87,90-92,94-100,103,104,106-110,113-115 and 117-119* is/are rejected.

7)☒ Claim(s) *77,78,88,89,101,102,111,112 and 120-123* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 109 is objected to because of the following informalities: The phrase "the first port of the transistor" is suggested to be changed to "the gate, source, or drain" of the first transistor". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 75, 79, 81, 83, 85, 86, 90, 92, 94, 96, 97, 98, 99, 106, 108, 109, 113, and 115, 117 and 119 are rejected under 35 U.S.C. 102(e) as being anticipated by Abou-Allam et al. (U. S. Patent No. 6, 094, 084).

Regarding claim 75, Abou-Allam et al. discloses an apparatus (Fig. 3, column 5, lines 23-column 7, line 5) for down-converting an electromagnetic signal, wherein an RF signal is an electromagnetic signal, comprising:

a capacitor (Fig. 3, element C1) having a first and second port;

a transistor (Fig. 3, element P3) having a source, gate, and drain; and

a resonant structure having a first and second port (Fig. 3, block 10);

wherein the first port of the capacitor (Fig. 3, element C1) is electrically coupled one of the source or drain of the transistor (D3), and the first port of the resonant structure (Fig. 3, block 20) is electrically coupled to the other of the source or drain of the transistor (S3); and

wherein a control signal (Fig. 2, LO) is electrically coupled directly to the gate of the transistor (G3), and an RF source signal (Fig. 3, Vin) is electrically coupled to the first port of the resonant structure (Fig. 3, block 10).

Regarding claim 79, which inherits the limitations of claim 75, Abou-Allam et al. discloses the first port of the capacitor (Fig. 3, element C1) is electrically coupled to an impedance matching network (Fig. 3, L6 and L7, column 6, lines 8-16).

Regarding claim 81, which inherits the limitations of claim 75, Abou-Allam et al. discloses the first port of the resonant structure (Fig. 3, block 10) is coupled to an impedance matching network (Fig. 3, elements L6 and L7).

Regarding claim 83, which inherit the limitations of claim 75, Abou-Allam et al. discloses the transistor is a FET (column 5, lines 25-53), wherein a p-channel MOS transistor is a FET transistor.

Regarding claim 85, which inherit the limitations of claim 75, Abou-Allam et al. discloses the transistor is a MOSFET (column 5, lines 25-53), wherein a p-channel MOS transistor is a MOSFET transistor.

Regarding claim 86, Abou-Allam et al. discloses an apparatus (Fig. 3, column 5, lines 23-column 7, line 5) for down-converting an electromagnetic signal, wherein an RF signal is an electromagnetic signal, comprising:

a first and second (Fig 3, elements C2 and C3) capacitor each having a first and second port;

a transistor (Fig. 3, element P3) having a source, gate, and drain; and

a resonant structure having a first and second port (Fig. 3, block 30);

wherein the first port of the first capacitor (C2) and the second port of the second capacitor (C3) are electrically coupled to one of the source or drain of the transistor (D3) wherein the second port of the second capacitor is coupled to the drain (D3) of the first transistor through the drain (D5) of a second transistor), and the first port of the second capacitor (C3) and the first port of the resonant structure (Fig. 3, block 30) are electrically coupled to the other of the source and the drain of the transistor (P3); and

wherein a control signal (Fig. 3, LO) is electrically coupled directly to gate of the transistor, and an RF source signal (Fig. 3, Vin) is electrically coupled to the first port of the resonant structure, and

Regarding claims 90, 92, 94 and 96, which inherit the limitations of claim 86, the claimed device includes features corresponding to subject matter mentioned above in the rejection of claims 79, 81, 83 and 85 which is applicable hereto.

Regarding claim 97, Abou-Allam et al. discloses an apparatus (Fig. 3, column 5, lines 23-column 7, line 5) for down-converting an electromagnetic signal, wherein an RF signal is an electromagnetic signal, comprising:

a capacitor (Fig. 3, element C1) having a first and second port;

a first and second transistor (Fig. 3, elements P4 and P5) each having a gate, drain, and source; and

wherein the first port of the capacitor (C1) is electrically coupled to one of the drain (D4) or source of the first transistor (P4), and the second port of the capacitor (C1) is electrically coupled to the one of the drain (D4) or source of the second transistor(P5), and the gate (G4) of the first transistor is electrically coupled to the gate (G5) of the second transistor; and

wherein a control signal (LO) is electrically coupled directly to the gate of the first transistor and the gate of the second transistor, and an RF source signal (Vin) is electrically coupled to the other of the drain or source (S4) of the first transistor and the other of the drain or source (S5) of the second transistor.

Regarding claim 98, which inherits the limitations of claim 97, Abou-Allam et al. discloses a resonant structure having a first and second port (Fig. 1, block 20),

wherein the first port of the resonant structure is electrically coupled to the other of the drain or source (S4) of the first transistor (P4) and second port of the resonant structure is coupled to the other of the drain (D5) or source of the second transistor (P5).

Regarding claim 99, which inherits the limitations of claim 98, Abou-Allam et al. discloses a first and second impedance each having a first and second port (elements L6 and L7),

wherein the first port of the first impedance (L6) is electrically coupled to the first port of a resonant structure (Fig. 3, block 20) and the first port of the second impedance (L7) is coupled to the second port of the resonant structure (block 20), and

wherein an RF source signal (Vin) is electrically coupled to the second port of the first impedance and the second port of the second impedance.

Regarding claims 106, which inherit the limitations of claim 97, Abou-Allam et al. discloses the transistors are FETs (column 5, lines 25-53), wherein a p-channel MOS transistor is a FET transistor.

Regarding claim 108, which inherit the limitations of claim 97, Abou-Allam et al. discloses the transistors are MOSFETs (column 5, lines 25-53), wherein a p-channel MOS transistor is a MOSFET transistor.

Regarding claim 109, Abou-Allam et al. discloses an apparatus (Fig. 3, column 5, lines 23-column 7, line 5) for down-converting an electromagnetic signal, wherein an RF signal is an electromagnetic signal, comprising:

a first and second (Fig. 3, elements C2 and C3) capacitor each having a first and second port;

a transistor (Fig. 3, element P3) having a source, gate, and drain; and

a load (Fig. 3, element R1L);

wherein the first port of the first capacitor (C2) and the first port of the second capacitor (C3) are electrically coupled to one of the source or drain (D3) of the transistor, the load (element R1L) and the second port of the second capacitor (C2) are electrically coupled to the other of the source (S3) and the drain of the transistor; and

wherein a control signal (Fig. 3, LO) is electrically coupled directly to gate of the transistor, and an RF source signal (Vin) is electrically coupled to the first port of the transistor.

Regarding claim 113, which inherits the limitations of claim 109, Abou-Allam et al. discloses the first port of the capacitor (C2) is electrically coupled to an impedance matching network (Fig. 3, elements L6 and L7).

Regarding claim 115, which inherits the limitations of claim 109, Abou-Allam et al. discloses the first port of the second capacitor (C3) is coupled to an impedance matching network (Fig. 3, elements L6 and L7).

Regarding claims 117, which inherit the limitations of claim 109, Abou-Allam et al. discloses the transistor is a FET FET (column 5, lines 25-53), wherein a p-channel MOS transistor is a FET transistor.

Regarding claim 119, which inherit the limitations of claim 109, Abou-Allam et al. discloses the transistor is a MOSFET (column 5, lines 25-53), wherein a p-channel MOS transistor is a MOSFET transistor.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 76, 80, 84, 87, 91, 95, 100, 103, 104, 107, 110, 114 and 118 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abou-Allam et al. (U. S. 6, 094, 084).

Regarding claims 76, 87, 100, 110, Abou-Allam et al. does not disclose a value of capacitance for the capacitor is selected so that the capacitor discharges stored energy to a load when the transistor is open. However, Abou-Allam et al. discloses the capacitance values are gate-source/drain capacitances of the transistors (column 6, lines 22-39) which are connected in series with a load (R1L and R2L). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that in order for the device to function properly the value of the capacitor would need to be correctly calculated for the capacitor to function properly. Thus, choosing a value for the capacitor is deemed a design choice and does not constitute patentability.

Regarding claims 80, 91, 103, 104 and 114, Abou-Allam et al. does not disclose the first port of the capacitor is electrically coupled to an amplifier or the first and second ports of the capacitor is electrically coupled to the first and second ports of a differential amplifier. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of an amplifier to amplify weaker signals which would allow more efficient processing.

Regarding claims 84, 95, 107, and 118, Abou-Allam et al. does not disclose the transistor is a JFET. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that since these are all transistors, that each of these devices could have been used to perform the switching function. Thus, choosing a type of transistor is deemed a design choice and does not constitute patentability.

Allowable Subject Matter

6. Claims 77, 78, 88, 89, 101, 102, 111, 112, and 120-123 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Andrys et al. (U. S. Patent No. 6, 057, 714) and Li et al. (U. S. Patent No. 5, 978,226) disclose downconversion circuits containing transistors, capacitors, and resonant circuits.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Curtis Odom
May 9, 2005

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